CLAIMS

What is claimed is:

1. A closed cell trench metal-oxide-semiconductor field effect transistor (TMOSFET) comprising:

a drain region;

a body region disposed above said drain region;

a gate region disposed within said body region;

a gate insulator region disposed about a periphery of said gate region;

a plurality of source regions disposed along the surface of said body region proximate a periphery of said gate insulator region;

wherein a first portion of said gate region and a first portion of said gate insulator region are formed as a substantially parallel elongated structure;

wherein a second portion of said gate region and a second portion of said gate insulator region are formed as a normal-to-parallel structure;

wherein a first portion of said drain region overlaps said parallel structure; and

wherein a second portion of said drain region is separated from said normal-to-parallel structure.

2. The closed cell TMOSFET according to Claim 1, wherein said closed cell MOSFET provides a low gate-to-drain capacitance (Cgd) on resistance (Rds-on) product.

3. The closed cell TMOSFET according to Claim 1, wherein said closed cell MOSFET provides a reduced gate-to-drain capacitance gate-to-source capacitance ratio.

4. The closed cell TMOSFET according to Claim 1, wherein said overlap of said first portion of said drain region and said parallel elongated structure comprises an extension of said drain region.

5. The closed cell TMOSFET according to Claim 1, wherein said separation of said second portion of said drain region and said normal-to-parallel elongated structure comprises a well of said body region.

6. The closed cell TMOSFET according to Claim 1, wherein said body region and said plurality of source regions are electrically coupled together.

7. The closed cell TMOSFET according to Claim 1, wherein;

said drain region comprises an n-doped semiconductor;

said body region comprises a p-doped semiconductor;

said gate insulator region comprises an oxide;

said plurality of source regions comprise a heavily n-doped semiconductor; and

said gate region comprises a heavily n-doped semiconductor.

8. The closed cell TMOSFET according to Claim 1, wherein said drain region comprises:

a first drain portion having a high doping concentration; and

a second drain portion, having a low doping concentration, disposed between said body region and said first drain portion.

9. The closed cell TMOSFET according to Claim 8, wherein said second drain portion increases a reverse breakdown voltage of said closed cell TMOSFET.

10. The closed cell TMOSFET according to Claim 8, wherein:

said first portion of said drain region comprises a heavily n-doped semiconductor; and

said second portion of said drain region comprises a lightly n-doped semiconductor.

11. A method of fabrication a closed cell trench metal-oxide-semiconductor field effect transistor (TMOSFET) comprising:

depositing a first semiconductor layer upon a substrate, wherein said first semiconductor layer is doped with a first type of impurity;

etching a plurality of trenches in said first semiconductor layer, wherein a first set of said plurality of trenches are substantially parallel with respect to each other and a second set of said plurality of trenches are normal-to-parallel with respect to said first set of said plurality of trenches;

forming a dielectric proximate said plurality of trenches;

doping said first semiconductor layer proximate the bottoms of said first set of said plurality of trenches;

depositing a second semiconductor layer in said plurality of trenches;

doping a first portion of said first semiconductor layer with a second type of impurity; and

doping a second portion of said first semiconductor layer proximate said dielectric with said first type of impurity.

12. The method according to Claim 11, wherein said depositing said first semiconductor layer comprises epitaxial depositing silicon lightly doped with phosphorous.

13. The method according to Claim 11, wherein said doping said first portion of said first semiconductor layer with said second type of impurity comprises implanting boron to form a body region.

14. The method according to Claim 11, wherein said forming a dielectric proximate said plurality of trenches comprises oxidizing said first semiconductor layer proximate said plurality of trenches.

15. The method according to Claim 11, wherein said etching said plurality of trenches is performed until the bottoms of said plurality of trenches reach a third portion of said first semiconductor layer.

16. The method according to Claim 15, wherein said doping said first semiconductor layer proximate the bottoms of said first set of said plurality of trenches comprises implanting boron to form a well surrounding a portion of said dielectric proximate the bottoms of said first set of said plurality of trenches.

17. The method according to Claim 16, further comprising doping said first semiconductor layer proximate the bottoms of said second set of said plurality of trenches with phosphorous to form an extension from said dielectric proximate the bottoms of the second set of said plurality of trenches to said third portion of said first semiconductor layer.

18. The method according to Claim 11, wherein said etching said plurality of trenches is stopped before the bottoms of said plurality of trenches reach a third portion of said first semiconductor layer.

19. The method according to Claim 18, wherein said doping said first semiconductor layer proximate the bottoms of said first set of said plurality of trenches comprises implanting phosphorous to form an extension from said dielectric layer proximate said bottoms of said first set of said plurality of trenches to said third portion of said first semiconductor layer.

20. The method according to Claim 19, further comprising forming a buried layer doped with boron from said dielectric layer proximate said bottoms of said second set of said plurality of trenches to said third portion of said first semiconductor layer.

21. The method according to Claim 11, wherein said depositing said second semiconductor layer in said plurality of trenches comprises chemical vapor depositing polysilicon heavily doped with phosphorous.

22. The method according to Claim 11, wherein said doping a second portion of said first semiconductor layer proximate said dielectric with said first type of impurity comprises implanting phosphorous to form a source region.

23. The method according to Claim 11, wherein said doping said first semiconductor layer proximate the bottoms of said first set of said plurality of trenches comprises implanting an impurity at a first angle such that said impurity is implanted in said first set of said plurality of trenches and not in said second set of said plurality of trenches.

24. A closed cell trench metal-oxide-semiconductor field effect transistor (TMOSFET) comprising:

a plurality of open gate-drain regions arranged in a first plurality of parallel regions; and

a plurality of closed gate-drain regions arranged in a second plurality of parallel regions normal to said open gate-drain regions.

25. The closed cell TMOSFET according to Claim 24, wherein the combination of said plurality of open gate-drain regions and said plurality of closed gate-drain regions reduces the gate-to-drain capacitance (Cgd) on resistance (Rds-on) product.

26. The closed cell TMOSFET according to Claim 24, wherein the combination of said plurality of open gate-drain regions and said plurality of closed gate-drain regions reduces the gate-to-drain capacitance gate-to-source capacitance ratio.